wherein the delay means comprises:

a comparator for comparing an edge of the clock signal, on which the data signal is intended to be latched, to at least one of leading and trailing edges of the data signal; and

a delay circuit for defining the delay time based on a result of comparison performed by the comparator, and

wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

9. (Amended) The input circuit of claim 4, wherein the first delay circuit defines the delay time based on the result of comparison performed by the comparator, between one of the leading edges of the data signal and the edge of the clock signal, and a setup time for correctly latching the data signal, and the second delay circuit defines the delay time based on the result of comparison performed by the comparator, between one of the trailing edges of the data signal and the edge of the clock signal, and the setup time for correctly latching the data signal.